WHAT IS CLAIMED IS:

1. A flip-flop comprising:

a mode configuration input for receiving a test enable signal for configuring the flip-flop between a test mode of operation and a normal mode of operation;

at least one data input for receiving at least one data signal, said flip-flop being capable of storing the at least one data signal when the flip-flop is in the normal mode of operation;

a scan input for receiving a test data signal, said flip-flop being capable of storing the test data signal when the flip-flop is in the test mode of operation;

a scan output; and

a circuit for enabling the scan output to output the logic value stored in the flip-flop when the flip-flop is in the test mode of operation and for disabling the scan output from outputting the logic value stored in the flip-flop when the flip-flop is in the normal mode of operation.

2. The flip-flop of claim 1, further comprising at least one latch, said circuit being coupled between the scan output and the at least one latch.

3. The flip-flop of claim 1, further comprising a data output for providing the value stored in the flip-flop, said circuit being coupled between the data output and the scan output.

4. The flip-flop of claim 3, wherein the circuit comprises at least one pass gate transistor coupled between the data output of the flip-flop and the scan output so that the scan output selectively follows the data output of the flip-flop.

5. The flip-flop of claim 1, wherein the circuit drives said scan output to a predetermined logic value when the flip-flop is in the normal mode of operation.

6. The flip-flop of claim 5, wherein the circuit comprises a pull down transistor coupled to the scan output for selectively driving the scan output to a low logic value.

7. The flip-flop of claim 5, wherein the circuit comprises a pull up transistor coupled to the scan output for selectively driving the scan output to a high logic value.

8. The flip-flop of claim 1, wherein the flip-flop is a D-flip-flop.

9. The flip-flop of claim 1, further comprising a data output for outputting the logic value stored in the flip-flop, wherein the circuit comprises a logic gate having a first input coupled to a data output of the flip-flop and an output coupled to the scan output for generating an output logic value.

10. The flip-flop of claim 9, wherein a second input of the logic gate is coupled to the mode configuration input.

11. An integrated circuit configured to operate in a normal mode of operation and a test mode of operation, said integrated circuit comprising:

a plurality of registers selectively connected together to form at least one serial shift register when the integrated circuit is configured in the test mode of operation, each of the registers including at least one flip-flop, said at least one flip-flop within each of the registers including at least a test enable input, a scan input, a data input, a scan output and a data output;

a combinational logic circuit for receiving as input the data output of the at least one flip-flop within a first of the registers and for generating a signal coupled to the data input of the at least one flip-flop within a second of the registers;

wherein the at least one flip-flop in each of the registers is enabled for storing the signal appearing on the scan input of the at least one flip-flop and disabled from storing the signal appearing on the data input of the at least one flip-flop when the integrated circuit is in the test mode of operation, disabled from storing the signal appearing on the scan input of the at least one flip-flop and enabled for storing the signal appearing on the data input of the at least one flip-flop when the integrated circuit is in the normal mode of operation, and enabled to output a logic value stored by the at least one flip-flop on the scan output of the at least one flip-flop when in the test mode of operation and disabled from outputting on the scan output the logic value stored by the at least one flip-flop when in the normal mode of operation.

12. The integrated circuit of claim 11, wherein said at least one flip-flop of each register comprises at least one pass gate transistor coupled between the data output and the scan output of the flip-flop for selectively providing, by the scan output, the logic value stored by the flip-flop.

13. The integrated circuit of claim 11, wherein the scan output of the at least one flip-flop of each register is driven to a predetermined logic value when in the normal mode of operation.

14. The integrated circuit of claim 13, wherein the at least one flip-flop of each register comprises a transistor coupled to the scan output for driving the scan output to the predetermined logic value.

15. The integrated circuit of claim 11, wherein the at least one flip-flop of each register comprises a logic gate having a first input coupled to a data output of the flip-flop, a second input of the logic gate coupled to the test enable input and an output coupled to the scan output.

16. A method for testing an integrated circuit having a plurality of registers therein, each one of the registers including at least one register bit having a scan output, said method comprising the steps of:

configuring the registers to form at least one serial shift register using the scan output of each register bit;

shifting a test pattern into the at least one serial shift register;

configuring the registers in a normal mode of operation, including disabling the scan output of at least some register bits so that for each of the at least some register bits, the scan output thereof is disabled from providing a value indicative of a value maintained by the register bit; and

applying at least one clock cycle to the registers.

17. The method of claim 16, wherein the step of configuring the registers in a normal mode of operation comprises the step of driving the scan output of at least some of the register bits to a predetermined logic value.

18. The method of claim 16, further comprising repeating the steps of configuring the registers to form at least one serial shift register chain, shifting, configuring the registers in a normal mode of operation, and applying the at least one clock cycle for different test patterns a number of times.

19. The method of claim 18, further comprising, following the step of repeating, the step of:

configuring the registers in a normal mode of operation, including disabling the scan output of the at least some register bits and driving the scan output to the predetermined logic value.

20. A method for operating a flip-flop having serial scan capabilities including a scan output, said method comprising the steps of:

receiving a mode configuration signal for configuring the flip-flop between a test mode of operation and a normal mode of operation; and

selectively disabling the scan output from providing the logic value stored by the flip-flop based upon the value of the mode configuration signal received.

21. The method of claim 20, further comprising:

selectively driving the scan output to a predetermined logic value based upon the value of the mode configuration signal received.

22. The method of claim 21, wherein the step of driving comprises driving the scan output to a low logic value.

23. The method of claim 21, wherein the step of driving comprises driving the scan output to a high logic value.

24. The flip-flop of claim 20, wherein the logic value stored in the flip-flop corresponds to an output of the flip-flop.

25. The flip-flop of claim 20, wherein the step of selectively disabling is performed when said mode configuration signal configures the flip-flop in the normal mode of operation.